

**REMARKS**

Claims 1-4, 7-11 and 14-22 are pending in the present application. Claim 1 has been amended.

**Claim Rejections-35 U.S.C. 102**

Claims 1, 2, 9, 12 and 16-18 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Sony reference (Japanese Patent Publication No. 2000-133572). This rejection is respectfully traversed for the following reasons.

The Examiner is respectfully requested to acknowledge that claim 12 has been cancelled, and thus should not be included with this rejection.

The Sony reference was cited and provided by Applicant along with the Information Disclosure Statement filed on August 17, 2005. However, the English language translations of the Japanese Patent Publications as provided along with the above noted Information Disclosure Statement were inadvertently misidentified and associated with the wrong references. That is, the English language translation identified at the top of the first page as corresponding to Japanese Patent Application Laid-Open No. 2000-150358, is actually the English translation of the Sony reference (Japanese Patent Publication No. 2000-133572). Applicant regrets any inconvenience or confusion that may occur in view of this inadvertent oversight. The following comments are offered in view of the English language translation that corresponds to Japanese Patent Publication No. 2000-133572 (which is misidentified as for Japanese

Application Laid-Open No. 2000-150358).

The semiconductor device of claim 1 includes in combination a substrate which has a main surface; an alignment mark “which is formed on the main surface and which has a pattern, wherein the pattern in a plane view has a shape that is obtained by eliminating corners from a polygon”; and an oxidation prevention cover film “on the alignment mark and formed as having the pattern”. Applicant respectfully submits that the Sony reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that Fig. 4 of the Sony reference discloses the features of claim 1, including an oxidation prevention cover film 15/16 on the alignment mark and formed having a pattern 13. However, as described in paragraph [0037] of the English translation of the Sony reference, upper film 15 as shown in Figs. 3B and 4 is silicon dioxide. As further described in paragraph [0043] of the English language translation of the Sony reference, layer 16 as shown in Fig. 4 is a photoresist that has Rhine patterns 13 shown in Fig. 3A formed therein. Layers 15 and 16 in Fig. 4 of the Sony reference are not described or even remotely suggested as having oxidation prevention characteristics. The Sony reference as relied upon by the Examiner thus does not disclose or even remotely suggest an oxidation prevention cover film on an alignment mark. More particularly, the Sony reference does not disclose or even remotely suggest an oxidation prevention cover film on an alignment mark and formed as having the pattern of the alignment mark, as would be necessary to meet the features of claim 1. Applicant therefore respectfully submits that the semiconductor

device of claim 1 distinguishes over the Sony reference as relied upon by the Examiner, and that this rejection of claims 1 and 2 is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination a substrate; an alignment mark; and an oxidation prevention cover film “on the alignment mark and formed as having the first through fourth sub-patterns”.

As emphasized above, the Sony reference as relied upon by the Examiner does not disclose or remotely suggest an oxidation prevention cover film on an alignment mark, and more particularly does not disclose or suggest an oxidation prevention cover film on an alignment mark and formed as having first through fourth sub-patterns, as would be necessary to meet the features of claim 9. Applicant therefore respectfully submits that the semiconductor device of claim 9 distinguishes over the Sony reference as relied upon by the Examiner, and that this rejection of claim 9 is improper for at least these reasons.

The semiconductor device of claim 16 includes in combination a substrate; an alignment mark; and an oxidation prevention cover film “on the alignment mark, wherein the oxidation prevention cover film is strip-like and has annular shape along another plane parallel to the main surface of the substrate”.

As emphasized above, the Sony reference as relied upon by the Examiner does not disclose an oxidation prevention cover film on an alignment mark. Moreover, even if silicon dioxide layer 15 and photoresist layer 16 could somehow be interpreted as an oxidation prevention cover film (which Applicant does not concede), layers 15 and 16 in

Fig. 4 of the Sony reference appear to be planar layers formed over the entirety of substrate 14. Layers 15 and 16 in Fig. 4 of the Sony reference are not strip-like, and do not have annular shape along another plane, as would be necessary to meet the features of claim 16. Applicant therefore respectfully submits that the semiconductor device of claim 16 distinguishes over the Sony reference as relied upon by the Examiner, and that this rejection of claims 16-18 is improper for at least these reasons.

**Claim Rejections-35 U.S.C. 103**

Claims 3, 7, 8, 10, 14, 15, 19, 20 and 22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sony reference. This rejection is respectfully traversed for the following reasons.

As noted above, the Sony reference as relied upon by the Examiner does not disclose or even remotely suggest an oxidation prevention cover film. The Sony reference as herein relied upon does not overcome the above noted deficiencies. Applicant therefore respectfully submits that claims 3, 7, 8, 10, 14, 15, 19, 20 and 22 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection is improper for at least these reasons.

With further regard to claim 7, since the Sony reference does not disclose or remotely suggest an oxidation prevention cover film, the Sony reference clearly would not make obvious a width of a pattern of an oxidation prevention cover film that is 1 micron to several micron wider at one side than a width of a pattern of an alignment

mark, as would be necessary to meet the features of claim 7. Applicant therefore respectfully submits that the semiconductor device of claim 7 would not have been obvious in view of the prior art as relied upon for at least these additional reasons. Applicant also respectfully submits that claims 14 and 20 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons.

Regarding claims 8, 15 and 22, since the Sony reference does not disclose or even remotely suggest an oxidation prevention cover film, the Sony reference clearly fails to make obvious an iridium-based metal oxidation prevention cover film as featured. Applicant therefore respectfully submits that claims 8, 15 and 22 would not have been obvious in view of the Sony reference as relied upon for at least these additional reasons.

Claims 4, 11 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Sony reference, in view of the Sato reference (Japanese Patent Publication No. 2002-64055). Applicant respectfully submits that the Sato et al. reference as herein relied upon does not overcome the above noted deficiencies of the Sony reference, and that this rejection of claims 4, 11 and 21 is improper for at least these reasons.

### **Conclusion**

Applicant respectfully submits that claim 1 has been amended merely to correct

a minor typographical error, not to further distinguish over any of the cited prior art.

Accordingly, the amendment of claim 1 should not be construed as narrowing scope within the meaning of *Festo*.

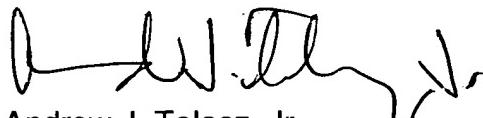
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.  
Registration No. 33,581

One Freedom Square  
11951 Freedom Drive, Suite 1260  
Reston, Virginia 20190  
Telephone No.: (571) 283-0720  
Facsimile No.: (571) 283-0740